Plenary Talk I

Data Mining-based Prediction Paradigm and Its Applications in Design Automation

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Abstract

Data mining algorithms operate on a collection of samples. There are many algorithms for a variety of mining purposes. In this talk, we will cover some key learning approaches found useful in design automation applications. We will present a number of examples in applying data mining in test, verification and post silicon timing analysis and debug. In-depth discussion will focus on more exciting results obtained in the past 2-3 years.

In pre-silicon design, functional verification remains a key bottleneck. In a design cycle, the design evolves over time. Consequently, functional verification is an iterative process in which extensive simulation is run on a few relatively stable versions of the design. In this context, data mining can be employed in two applications, to reduce the simulation time required to find an important test and to improve a test template for generating additional important verification tests. First, we describe a novel test detection framework that can filter out a large number of unimportant tests before simulation, effectively reducing the simulation time by up to 90%. The data mining approach is based on novelty detection. We then discuss a feature-based analysis approach to extract special properties of novel tests. These properties are then used to improve the test template for achieving a better coverage. The data mining approach is feature-based rule learning. To validate the ideas, we show experimental results on a low-power 64-bit Power Architecture-based processor core.

For processor design, one important task in post-silicon is to identify speed limiting paths as guides for performance improvement. Data mining can be applied in two applications, facilitating the identification of potential speed paths and understanding known speed paths. Design issues were uncovered by analyzing top speed paths against a large number of non-speed paths, which otherwise were difficult to find without the proposed feature-based data mining approach.

In IC production, test cost and/or quality continue to be major concerns. We will discuss how to predict potential defective parts as novel samples. Because novelty depends on the tests used in the analysis, we will also discuss the test selection problem. Caser studies discussed are based on real industrial test data from SoC production lines for the automotive market where quality requirement is extremely high.

Higher quality usually demands more sophisticated test processes and hence, higher cost. One expensive test process that contributes significantly to the cost of an IC is the burn-in

process. We will address potential burn-in cost reduction by using data mining techniques to predicting part that do not need long hours of burn-in.

Biography

Dr. Magdy S. Abadir received the B.Sc. degree with honors in Computer Science and Automatic Control from the University of Alexandria, Egypt in 1978, the M.Sc. degree in Computer Science from the University of Saskatchewan, Saskatoon, Canada, in 1981, and the Ph.D. degree in Electrical Engineering from the University of Southern California, Los Angeles, in 1986.

Currently he is an independent consultant and a member of the board of directors of a number of EDA companies. Prior to that he spent almost 20 years with Freescale/Motorola in various roles. His last position was the Director of Design Automation, Technology Solutions Organization, Prior to joining Motorola he was the General Manager of Best IC Labs in Austin Texas. From 1986 to 1994 he worked at the Microelectronics and Computer Technology Corporation (MCC) in Austin Texas.

Dr. Abadir has been selected in 2005 as an IEEE fellow for contribution in the verification and test of microprocessors. He has 10 patents issued plus several that has been filed. He co-founded and chaired a series of international workshops on the economics of design, test and manufacturing, and on microprocessor test and verification (MTV). He has co-edited several books on those subjects, and he also published over 300 technical journal and conference papers in the areas of test economics, design for test, and design verification and economics. Four of his papers received best paper awards (DATE 98, ASP-DAC 2002, DATE 2003, and VLSI-DAT 2011). Dr. Abadir also served as an adjunct faculty at the University of Texas at Austin.